

WORLD INTELLECTUAL PROPERTY ORGANIZATION  
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The diagram illustrates the TTPB system architecture, enclosed in a dashed box. The components and their interconnections are as follows:

- PL (Program Loader)**: Connected to the **LI (Local Interface)** and the **CU (Control Unit)**.
- LI (Local Interface)**: Connected to the **CU** and the **EU (Execution Unit)**.
- LS (Local Storage)**: Connected to the **CU**.
- CU (Control Unit)**: The central control component, connected to the **LI**, **LS**, **EU**, and the **CDR (Control Data Register)**.
- CDR (Control Data Register)**: A vertical stack of three registers labeled **D**, **C**, and **S**. Each register has a bidirectional arrow pointing to the **CU**.
- RTC (Real-Time Clock)**: Connected to the **D** register of the **CDR**.
- GU (Global Unit)**: Connected to the **C** register of the **CDR** and the **SRN (Serial Random Number Generator)**.
- SRN (Serial Random Number Generator)**: Connected to the **S** register of the **CDR** and the **PCR (Program Counter)**.
- PCR (Program Counter)**: Connected to the **EU** and the **SRN**.
- EU (Execution Unit)**: The main processing unit, connected to the **CU**, **LI**, **PCR**, and the **DATA** and **H-DATA** buses.
- DATA and H-DATA Buses**: These buses connect the **EU** to the **RD (Random Data)** block outside the dashed box.